Amendments to the Claims:

1. (Currently Amended) A system of controlling and triggering a TRIAC (TR), the TRIAC comprising a gate (G), the TRIAC (TR) being connected to a load, the gate (G) being electrically connected to a power unit that actuates the TRIAC (TR) for selectively applying a network voltage (V_{AC}) to the load and enabling the circulation of an electric current (i_c) in the load, the system comprising:

- a voltage detection unit for detecting gate voltage;
- a detection unit for detecting passage of the feed network voltage by zero;
- a power unit; and
- a control unit;

the voltage detection unit being electrically connected to the control unit,

the control unit establishing an adjustable gate (G) voltage limit value (+limit, -limit), and generating a pulse at the gate (G) of the TRIAC (TR) to keep it in conduction,

the pulse at the gate (G) being generated from a comparison between the voltage limit value (+limit, -limit) established by the control unit and a voltage measured at the gate (G) from the gate voltage detection unit,

the detection unit for detecting voltage at the gate (G) comprising a comparator (CP_1) electrically connected to the gate (G) of the TRIAC (TR) and to a digital-to-analog (D/A) converter, the comparator (CP_1) receiving the signal of the voltage at the gate (G) of the TRIAC (TR) and a signal generated by the D/A converter, the D/A converter receiving a digital signal generated by a control central, the signal generated by the control central establishing an adjustment voltage value, the adjustment voltage value being equal to the limit values (+limit, -limit),

the power unit being associated to the control unit and generating a voltage pulse at the gate of the TRIAC (TR) upon a command from the control central,

wherein the voltage of the gate (G) of the TRIAC (TR) is applied to the comparator (CP) by means of a resistive divider (R_1, R_2), and wherein the resistive divider (R_1, R_2) is formed by resistors of the same value.

2. (Previously Presented) A system according to claim 1, wherein the control unit measures the electric current (i_c) and adjusts the voltage limit value (+limit, -limit) in a proportional way to the current (i_c) value measured.

3. (Previously Presented) A control system according to claim 2, wherein the control unit generates the pulse at the gate (G) of the TRIAC (TR) in previously established a measurement time (t_M), the measurement time (t_M) occurring before passage of the current (i_c) by zero.

4. (Previously Presented) A system according to claim 2, wherein the control unit obtains the current (i_c) value from a current sensor.

5. (Previously Presented) A system according to claim 2, wherein the adjustment of the limit value (+limit, -limit) is made by means of the equation: $\pm Limit = k \times I_c$, wherein k is a previously determined proportionality constant.

6. (Previously Presented) A system according to claim 2, wherein the adjustment of the limit (+limit, -limit) is made by means of a table of preestablished values stored in the control unit.

7. (Canceled).

8. (Canceled).

9. (Previously Presented) A system according to claim 7, wherein the control unit comprises a digital-to-analog (D/A) converter, the digital-to-analog converter generating the adjustment voltage value.

10. (Previously Presented) A system according to claim 8, wherein the pulse at the TRIAC (TR) is generated when the control central detects a transition of level of the comparator (CP_1) output.

11. (Previously Presented) A system according to claim 8, wherein the control central commands the digital-to-analog (D/A) converter to commute between a positive voltage limit

(+limit) to a negative limit (- limit) and vice-versa at every transition received by the comparator (CP_1).

12. (Canceled).

13. (Canceled).

14. (Previously Presented) A system according to claim 7, wherein the digital-to- analog (D/A) converter is internal with respect to the control central.

15. (Previously Presented) A system according to claim 7, wherein the comparator (CP_1) is internal with respect to the control central.

16. (Previously Presented) A system according to claim 7, wherein the power control unit is an internal switch of the control central.

17. (Currently Amended) A method of controlling the triggering of a TRIAC (TR), the TRIAC comprising a gate (G) and being electrically connected to a network voltage (V_{AC}),

the TRIAC (TR) being selectively actuated upon a pulse at the gate (G) to apply the network voltage (V_{AC}) to a load, enabling the circulation of a current (ic),

a single comparator (CP_1) being associated to the gate (G) of the TRIAC (TR),

the method comprising:

applying a pulse at the gate (G) when the voltage limit value (+limit, - limit) at the gate (G) has been detected, the pulse being generated from a transition at the comparator (CP_1), the comparator (CP_1) comparing the voltage limit value (+limit, -limit) at the gate (G) and a voltage measured at the gate (G), wherein the voltage measured at the gate (G) of the TRIAC (TR) is applied to the comparator (CP_1) by means of a resistive divider (R_1, R_2), and wherein the resistive divider (R_1, R_2) is formed by resistors of the same value,

commuting an input of the comparator (CP_1) from the positive voltage limit (+limit) to a negative limit (-limit) and vice-versa at every transition received by the comparator (CP_1).

18. (Previously Presented) A method according to claim 17, wherein, prior to the step of applying the pulse at the gate (G), said method comprises the steps of:

measuring the current (i_c) circulating in the load, and

adjusting the level of the voltage value at the gate (+limit, -limit) proportional to the level of the current (i_c)

19. (Previously Presented) A method according to claim 18, wherein, in the step of adjusting the voltage limit value (+limit, -limit), the equation: $\pm Limit = k \, x \, i_c$ is applied, wherein k is a proportionality constant.

20. (Previously Presented) A method according to claim 18, wherein, in the step of adjusting the voltage limit value (+limit, -limit), there is a step of reading a table of pre-established values.

21. (Previously Presented) A method according to claim 18, wherein the voltage pulse at the gate (G) has a duration sufficient for the current circulating in the TRIAC (TR) to reach a latch value.

22. (Previously Presented) A method according to claim 21, wherein the first pulse of the gate (G) is commanded from a measurement of passage of the network (V_{AC}) by zero.

23. (Currently Amended) A method of controlling the triggering of a TRIAC (TR), the TRIAC comprising a gate (G) and being electrically connected to a network voltage (V_{AC}),

the TRIAC (TR) being selectively actuated upon a pulse at the gate (G) to apply the network voltage (V_{AC}) to a load, enabling the circulation of a current (i_c),

the method comprising the steps of:

applying a pulse at the gate (G) when the current value (i_c) reaches a minimum value, establishing a voltage limit value (+limit,-limit) at the gate (G) to generate the pulse at the gate (G) of the TRIAC (TR) for keeping it in conduction, the pulse at the gate (G) being generated in a previously established measurement time (t_M), the measurement time (t_M) occurring before passage of the level of the current (i_c) by zero, comparing the voltage limit value (+limit,-limit)

to the voltage of the gate (G) to determine when to apply the pulse, wherein the voltage of the gate (G) of the TRIAC (TR) is applied to the comparator (CP) by means of a resistive divider (R_1, R_2) formed by resistors of the same value,

measuring the current (i_c) that circulates in the load, and

adjusting the level of the voltage limit value (+limit, -limit) at the gate (G) by a control unit in a proportional way to level of the current (i_c).

24. (Previously Presented) A method according to claim 23, wherein the current (i_c) is continuously measured.

25. (Previously Presented) A method according to claim 24, wherein, in the step of applying the pulse at the gate (G) of the TRIAC (TR_1), regulating the level of voltage in the load from the delay in generating the pulses at the gate (G).